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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/830,719	08/01/2001	Rowan Nigel Naylor	P16820US1	3645

27045　　　7590　　　09/11/2006	EXAMINER
ERICSSON INC. 6300 LEGACY DRIVE M/S EVR C11 PLANO, TX 75024	MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/830,719	NAYLOR, ROWAN NIGEL
	Examiner	**Art Unit**	
	Tonia L. Meonske	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>19 June 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-26</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) <u>14-26</u> is/are allowed.

6)☒ Claim(s) <u>1-13</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-3, 5-9, 12 and 13 are rejected under 35 U.S.C. 102(b) as being

anticipated by Fu et al., US Patent 5,226,127 (Herein after "Fu".).

3.   Referring to claim 1, Fu has taught a processing arrangement for a computer,

the arrangement comprising:

     a.   a first processor means which is operable to process instructions from a

first set of instructions (column 6, lines 37-49); and

     b.   a second processor means which is operable to process instructions from

a second set of instructions, which second set of instructions is a subset of the

first set of instructions (column 6, lines 37-49, Figure 1), the second processor

means being arranged to receive instructions and to process the received

instructions independently from the first processor means, when the received

instructions are selected from the second set of instructions (column 6, lines 37-

49, Instructions are either fully executed on the general purpose processor or the

special purpose processing unit (numeric coprocessor). Once the coprocessor

receives an instruction of it's subset, that instruction is independently executed,

meanwhile the general purpose processor is either actively executing other

instructions or in an inactive wait state.), wherein the first processor means

includes a plurality of registers, and the second processor means is operable to

access a predetermined, non-zero, selection of the said registers (Figure 1,

column 3, lines 39-49, The floating point co-processor will effect the same

registers that are affected by the general purpose processor.), and wherein the

first and second processor means are operable to process respective instructions

in parallel with one another (Column 3, line 50-column 4, line 7, When the main

processor does not wait for the coprocessor to complete processing the

respective instructions are executed in parallel.).

4.   Referring to claim 2, Fu has taught the processing arrangement of claim 1, as

described above, and wherein the first processor means has active and inactive

states of operation (column 2, line 65-column 4, line 7, column 5, lines 12-17, The

general purpose processor is either actively executing instructions or in an inactive wait

state.), and wherein the second processor means is operable to process instructions

when the first processor means is in the inactive state (column 2, line 65-column 4, line

7, column 5, lines 12-17, The numeric processor executes instructions while the main

processor is in a wait state.).

5.   Referring to claim 3, Fu has taught the processing arrangement of claim 2, as

described above, and wherein the second processor means is operable to cause the

first processor means to change to the active state from the inactive state, when the

received instructions cannot be processed by the second processor means (column 2,

line 65-column 4, line 7, column 5, lines 12-17, "Active state" is interpreted as currently

executing instructions. "Inactive state" is interpreted as not currently executing any

instructions. In synchronization wait state no other instructions can be executed until

the coprocessor is available to execute other instructions.).

6.   Claim 5 has nothing over claim 1 and is rejected for the same reasons as set

forth in claim 1.

7.   Claim 6 has nothing over claim 2 and is rejected for the same reasons as set

forth in claim 2.

8.   Referring to claim 7, Fu has taught a computer processing arrangement, the

arrangement comprising:

      a.   a host processor (column 6, lines 37-49), including a plurality of registers

(Figure 1, column 3, lines 39-49), operable to process instructions from a first set

of instructions (column 6, lines 37-49); and

      b.   a shadow processor (column 6, lines 37-49) operable to access a

predetermined, non-zero, selection of the registers (Figure 1, column 3, lines 39-

49, The floating point co-processor will effect the same registers that are affected

by the general purpose processor.) and to process instructions from a second set

of instructions, which second set of instructions is a subset of the first set of

instructions (column 6, lines 37-49); and

      c.   wherein the second set of instructions used by the shadow processor is

selected from a group consisting of servicing multiple tasks (column 3, lines 56-

68, column 5, lines 12-17) and exceptions (column 3, lines 62-64), maintaining

contexts of the host processor (column 3, lines 60-63), and controlling interrupts

received from peripherals coupled to the computer (column 3, lines 65-67).

9.   Claim 8 and 9 have nothing over claims 3 and 4 and are therefore rejected for

the same reasons as set forth in claims 3 and 4.

10.   Referring to claim 11, Fu has taught the computer processing arrangement of

claim 10, as described above, and wherein each such shadow processor is one from

the group consisting of a RISC CPU, a logic processor (column 6, lines 37-49, All

processors are logic processors since low-level logic gates are used to implement

processors.) and a memory management processor (Only one processor from the

group needs to be in the reference to read on the claim as worded.).

11.   Referring to claim 12, Fu has taught a method of operating a computer having

a first processor that operates to process instructions from a first set of instructions

(column 6, lines 37-49), and a second processor that operates to process instructions

from a second set of instructions, the second set of instructions being a subset of the

first set of instructions (column 6, lines 37-49), the method comprising the steps of:

using the second processor to receive instructions; and processing the received

instructions using the second processor independently from the first processor when the

received instructions are selected from said second set of instructions (column 6, lines

37-49, Instructions are either fully executed on the general purpose processor or the

special purpose processing unit (numeric coprocessor). Once the coprocessor receives

an instruction of it's subset, that instruction is independently executed, meanwhile the

general purpose processor is either actively executing other instructions or in an

inactive wait state.), wherein the first processor includes a plurality of registers (Figure

1, column 3, lines 39-49), and the second processor is operable to access a

predetermined, non-zero selection of the registers (Figure 1, column 3, lines 39-49, The

floating point co-processor will effect the same registers that are affected by the general

purpose processor.), and wherein the second set of instructions used by the second

processor is one selected from the group consisting of servicing multiple tasks (column

3, lines 56-68, column 5, lines 12-17) and exceptions (column 3, lines 62-64),

maintaining contexts of the first processor (column 3, lines 60-63), and controlling

interrupts received from peripherals coupled to the computer (column 3, lines 65-67).

12.   Claim 13 has nothing over claim 2 and is rejected for the same reasons as set

forth in claim 2.

Claim Rejections - 35 USC § 103

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a)   A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to be patented
> and the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

14.   Claims 4, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Fu et al., US Patent 5,226,127 (Herein after "Fu".).

15.   Referring to claim 4, Fu has taught the processing arrangement of claim 3, as

described above. Fu has not specifically taught further comprising a plurality of

processing arrangements having a plurality of second processor means and a plurality of

corresponding first processor means wherein each second processor means is

operable to cause the corresponding first processor means to change to the active state

from the inactive state, when the received instructions cannot be processed by the its

corresponding second processor means for processing respective subsets of the first

instruction set. However, duplicating a part for multiple effect has been held to be an

unpatentable difference. *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA

1960). This claim is merely duplicating the claimed first and second processors.

Increasing the number of processors in the system would have increased the overall

instruction processing parallelism of the processor. Therefore it would have been

obvious to one of ordinary skill in the art at the time the invention was made to have the

processing arrangement of Fu comprise a plurality of processing arrangements having a

plurality of second processor means and a plurality of corresponding first processor

means wherein each second processor means is operable to cause the corresponding

first processor means to change to the active state from the inactive state, when the

received instructions cannot be processed by the its corresponding second processor

means for processing respective subsets of the first instruction set, for the desirable

purpose of increasing instruction processing parallelism and since it has been held that

duplicating a part for multiple effect in not a patentable difference.

16.   Claim 10 has nothing over claim 4 and is rejected for the same reasons as set

forth in claim 4.

17.   Referring to claim 11, Fu has taught the computer processing arrangement of

claim 10, as described above, and wherein each such shadow processor is one from

the group consisting of a RISC CPU, a logic processor (column 6, lines 37-49, All

processors are logic processors since low-level logic gates are used to implement

them.) and a memory management processor (Only one processor from the group

needs to be in the reference to read on the claim as worded.).

Response to Arguments

18.   Applicant's arguments filed June 19, 2006 have been fully considered but they

are not persuasive.

19.   On page 8, Applicant argues in essence:

"in Fu, the microprocessor and the co-processor are described as both being in active states (e.g. the microprocessor is not in a sleep state while the co-processor is operating), although the microprocessor of Fu is waiting while the second processor is in operation. Thus, in Fu, there is a dependence of the co-processor on its corresponding microprocessor."

However, in claim 1 applicant has merely claimed "process the received

instructions independently from the first processor means". Applicant is

attempting to interpret claim 1 narrower than what is actually claimed. Fu has

taught to "process the received instructions independently from the first

processor means" (column 6, lines 37-49). In fu instructions are fully executed

either on the general purpose processor or the special purpose processing unit

(numeric coprocessor). Once the coprocessor receives an instruction of it's own

subset, that instruction is independently executed, meanwhile the general

purpose processor is either actively executing other instructions or in an inactive

wait state. In this case, at best, there is some level of dependence of the main

processor on the coprocessor. Since the coprocessor of Fu fully executes is own

received instructions, the coprocessor is not dependent on the main processor.

Therefore this argument is moot.

20.   Applicant's arguments with respect to claims 4-5 have been considered but are

moot in view of the new ground(s) of rejection.

Allowable Subject Matter

21.   Claims 14-26 are allowed.

Conclusion

22.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

23.   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

24.   Any inquiry concerning this communication or earlier communications from the

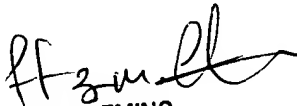examiner should be directed to Tonia L. Meonske whose telephone number is (571)

272-4170. The examiner can normally be reached on Monday-Friday with first Friday's

off.

25.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

26.   Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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9/5/2006